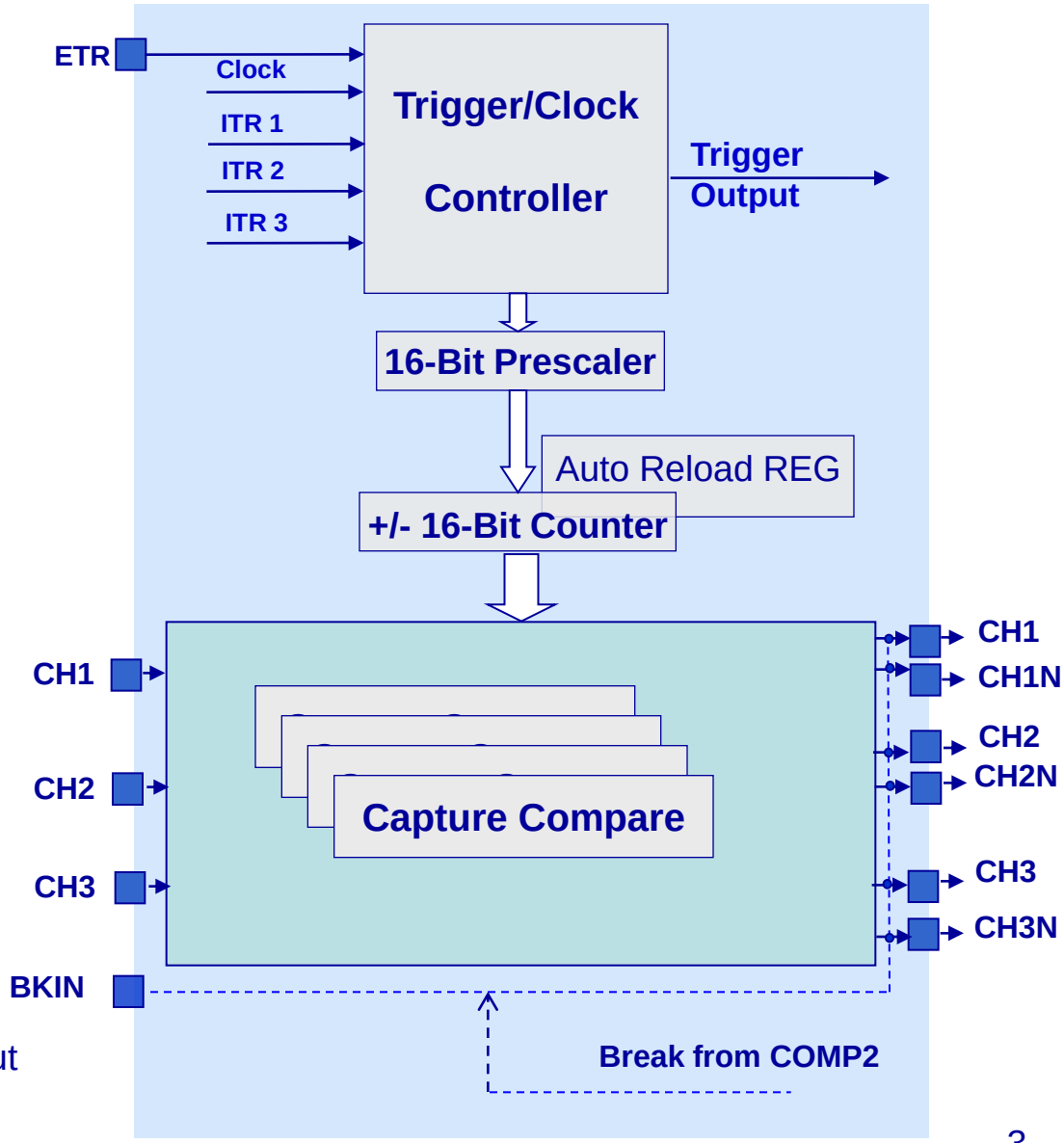
MMS – MCD
Application Team

STM8L Training Slides

Advanced Control And General Purpose Timers

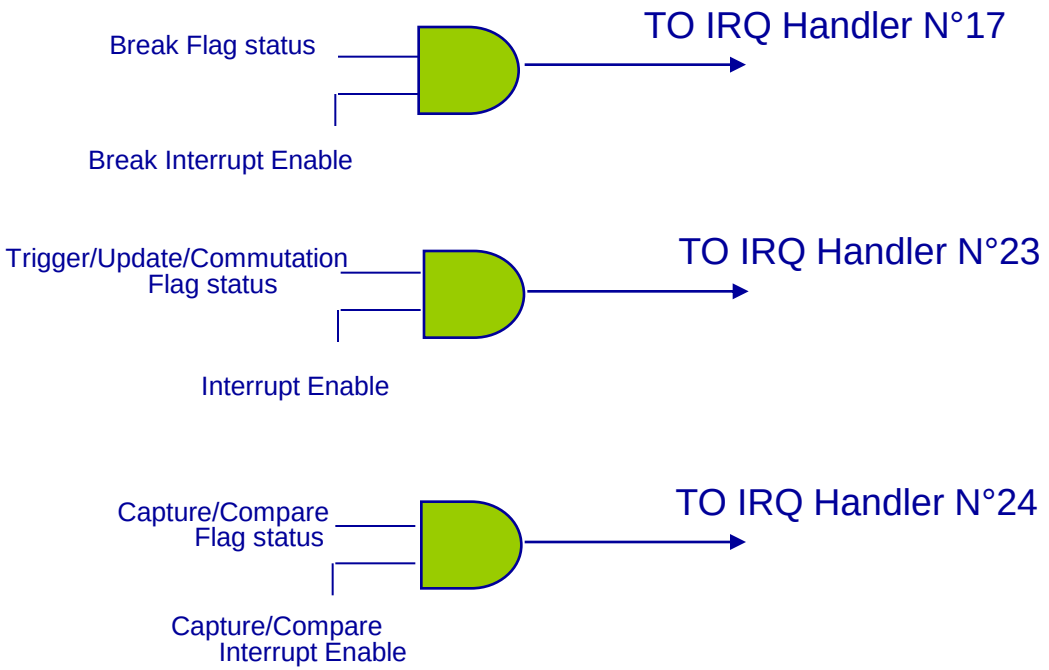
Features overview

- 16-bit Counter
  - Auto Reload
  - Up, down and center-aligned modes
- 4 x 16 High resolution Capture Compare channels
  - Programmable direction of the channel: input/output
  - Output Compare: Toggle, PWM
  - Input Capture
  - PWM Input Capture
- Synchronization between Timers
- Up to 8 interrupts and up to 6 DMA requests
- Motor Control Specific Features
- OC Signal Management
  - Complementary outputs on three channels
  - Dead-time management
  - Repetition Unit
- Encoder Interface
- Embedded Safety features
  - Break sources: BKIN pin / comparator 2 output
  - Lockable unit configuration



Interrupts request sources

- 8 Interrupt request sources mapped on 3 interrupt vectors:
  - Break input
  - Trigger event
  - Update event (overflow, underflow…)
  - Commutation event
  - Capture / compare 1 event
  - Capture / compare 2 event
  - Capture / compare 3 event
  - Capture / compare 4 event

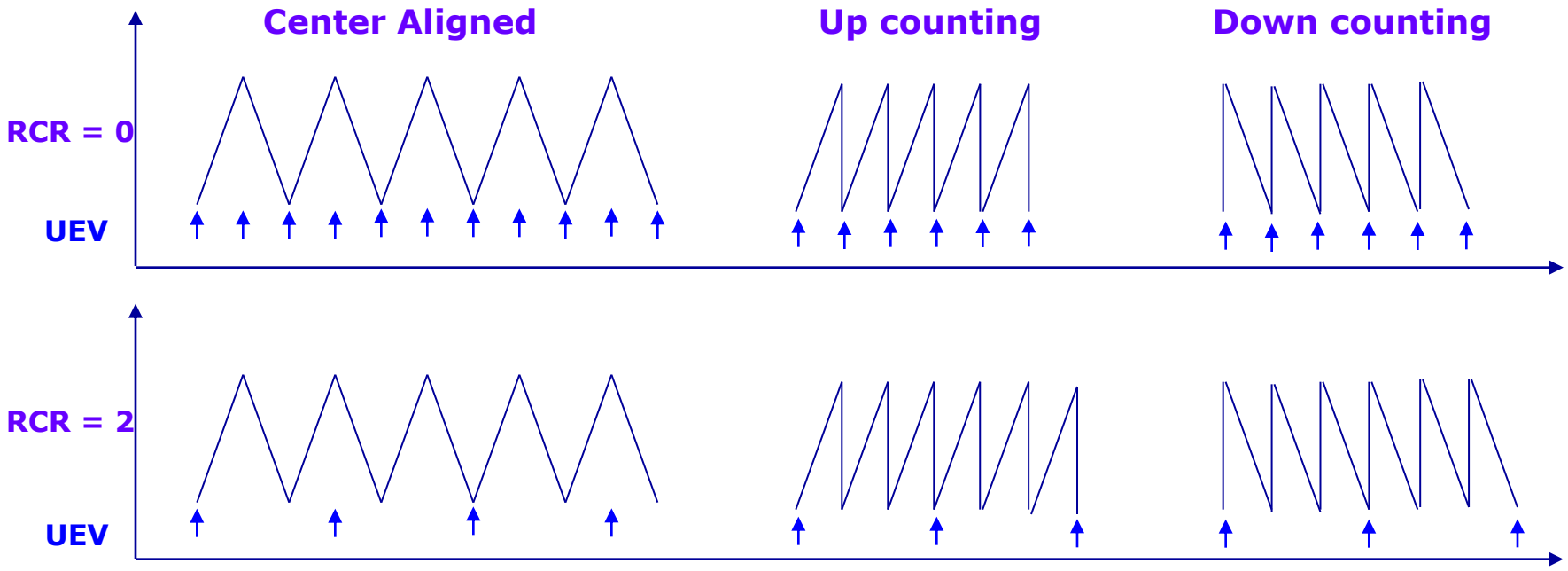


DMA capability

- 6 DMA request sources:
  - Commutation event
  - Capture / Compare 1 event
  - Capture / Compare 2 event
  - Capture / Compare 3 event
  - Capture / Compare 4 event
  - Update event (overflow, underflow…)
- 2 DMA modes:
  - Single mode: single register is transferred to or from a single TIM register
  - Burst mode: block of timer registers is transferred

Counter Modes

- There are three counter modes:
  - Up counting mode
  - Down counting mode
  - Center-aligned mode
- When using the Repetition Counter



Update Event

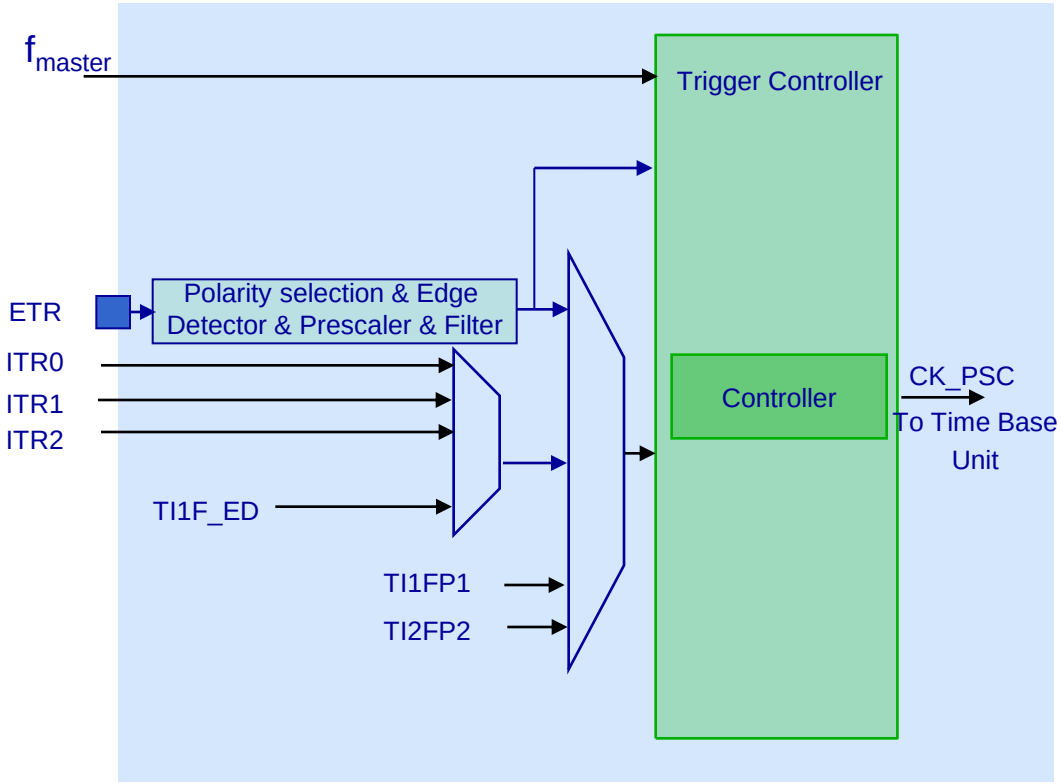
- The content of the preload register is transferred in the shadow register (depending on the auto-reload preload is enable or not):
  - immediately
  - at each update event (UEV)

- The Update Event is generated:
  - when the counter reaches overflow/underflow
  - when the Repetition counter equals to 0
  - by software by setting the Update Generation bit (UG)

- The Update event UEV requests can be selected as follow:
  - The requests are sent only when the counter reaches the overflow/underflow.
  - The requests are sent when:
    - Counter overflow/underflow
    - Update Generation bit (UG) is set
    - Update event is generated through the clock trigger controller

Counter Clock Selection

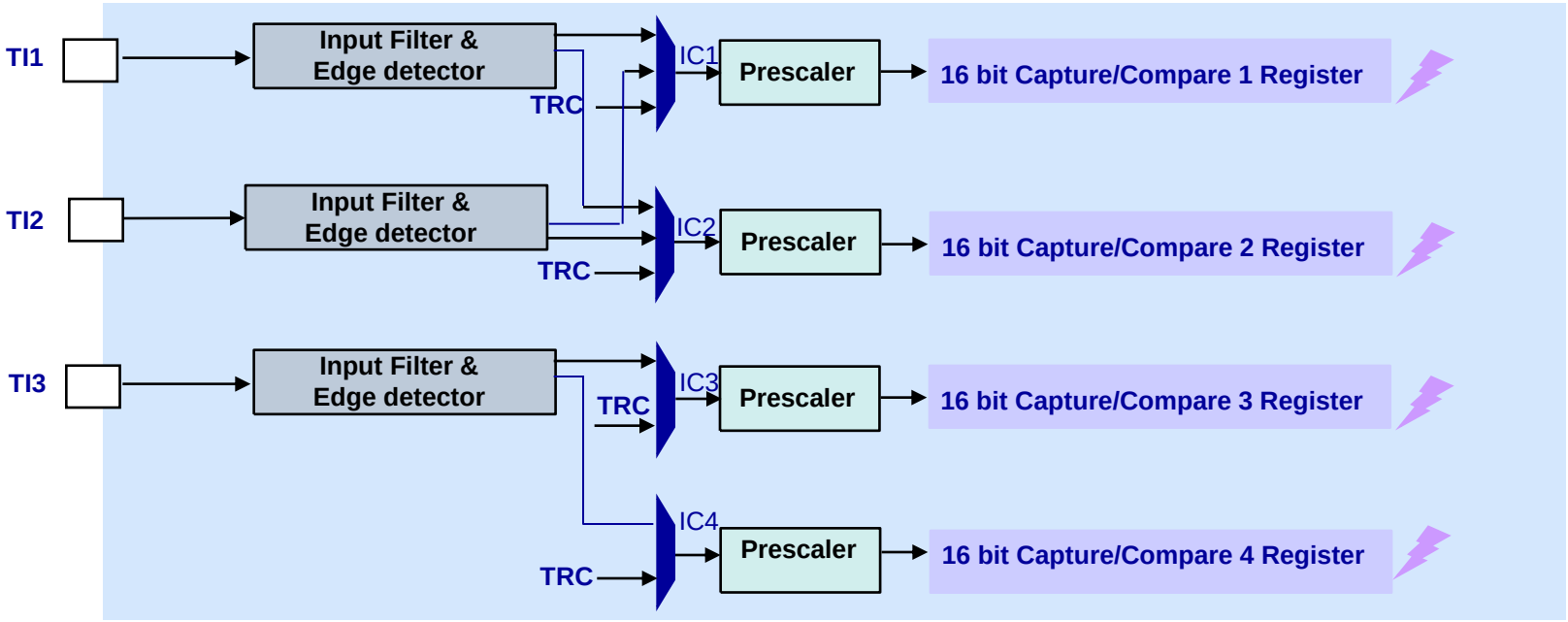
- Clock can be selected out of 8 sources:
  - Internal clock f_{sysclk} provided by the clock controller
  - Internal trigger input 1 to 3: ITR0, ITR1 or ITR2
  - External Capture Compare pins TI1FP1, TI1F_ED or TI2FP2
  - External trigger input ETR:
    - Programmable polarity
    - 4 bits External Trigger Filter
    - Prescaler: Division by 1, 2, 4 or 8



Capture Compare Array presentation

- The Capture Compare Array is composed of:
  - Capture Compare channels
  - Break functionality
- Programmable direction of each channel: input/output use
- Each Channel is composed of:
  - Capture/Compare register
  - Input stage for capture:
    - 4 bits digital filter
    - Edge detector
    - Input Capture prescaler (Capture done at each detected edge, every two edges, every 4 edges or every 8 edges)
  - Output stage for Compare:
    - Output mode controller
    - Dead Time generator

Input Capture Mode



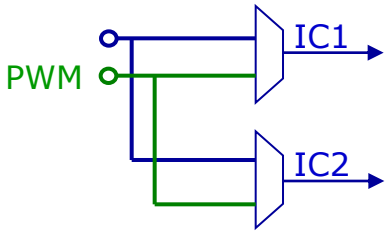
- IC1 and IC2 can be mapped on TI1 and TI2, IC3 and IC4 can be mapped only on TI3.
- 4x16-bit capture compare registers are programmable to be used to latch the value of the counter after a transition detected by the corresponding Input Capture.
- When a capture occurs, the corresponding CCxIF flag is set and an interrupt or a DMA request can be sent if they are enabled.
- Possible set of an over-capture flag If a capture occurs while the CCxIF flag was already high.

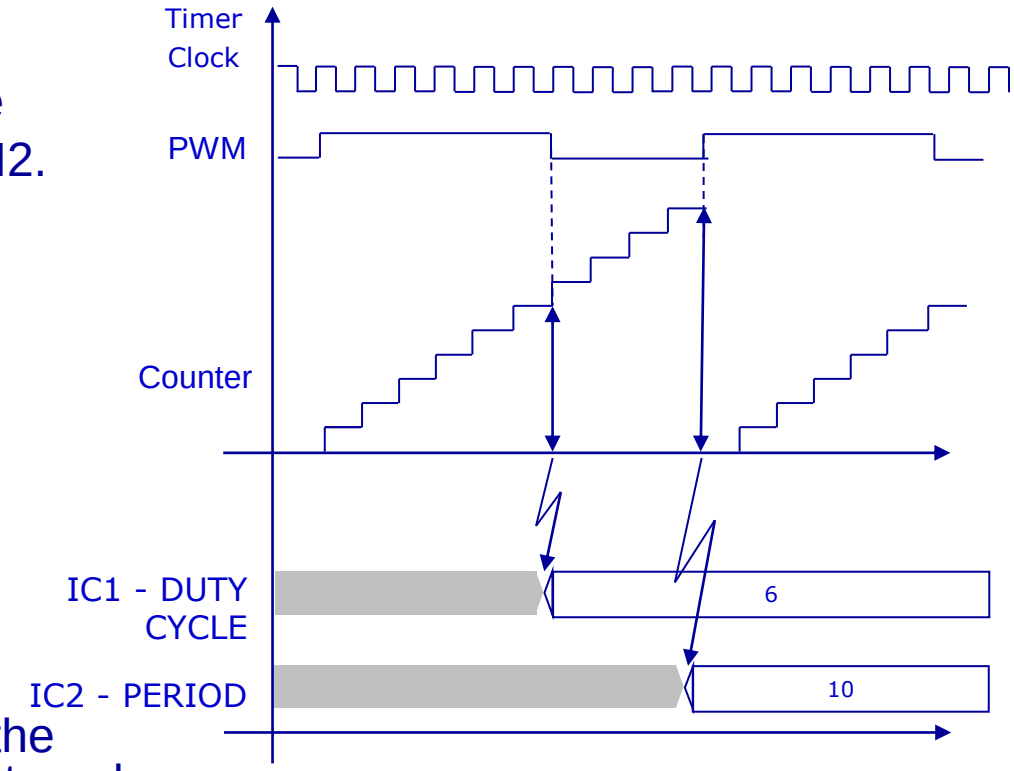
PWM Input Mode

PWM Configuration tips:

- IC1 and IC2 must be configured to be connected together to the PWM signal:

⇨ IC1 and IC2 are redirected internally to be mapped to the same external pin TI1 or TI2.



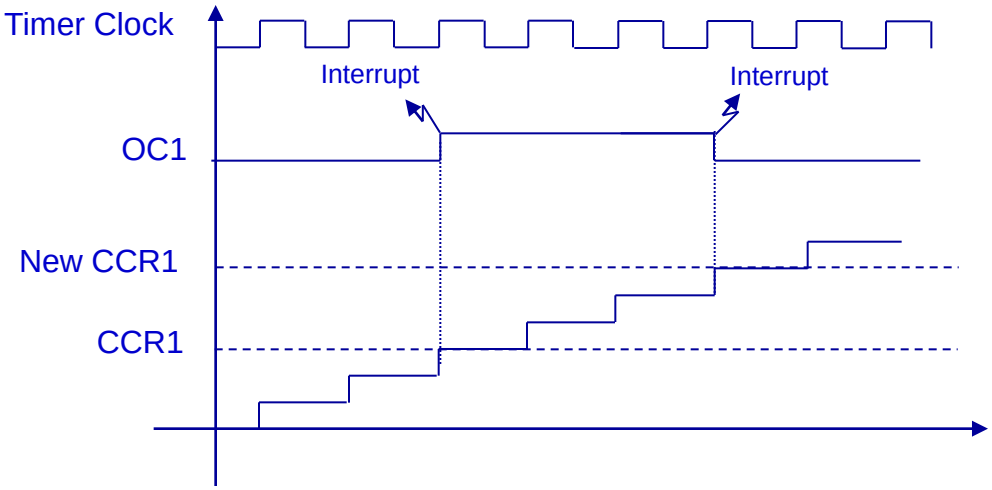


- IC1 and IC2 active edges must have opposite polarity.
- IC1 or IC2 is selected as trigger input and the clock/trigger controller is configured in reset mode.

The PWM Input functionality enables the measurement of the period and the pulse width of an external waveform.

Output Compare Mode

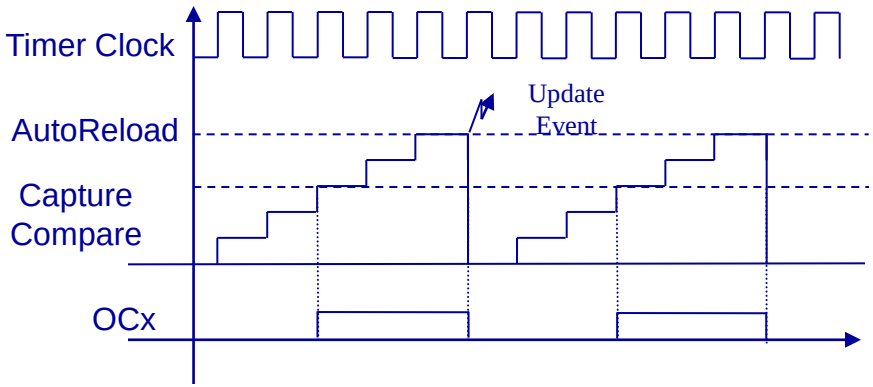
- The Output Compare is used to control an output waveform or indicate when a period of time has elapsed.
- When a match is found between the capture/compare register CCR and the counter:
  - The corresponding output pin is assigned to the programmable Mode, it can be:
    - Set
    - Reset
    - Toggle
    - Remain unchanged
  - Set a flag in the interrupt status register
  - Generates an interrupt if the corresponding interrupt mask is set
  - Send a DMA request if the corresponding enable bit is set
- The CCRx registers can be programmed with or without preload registers



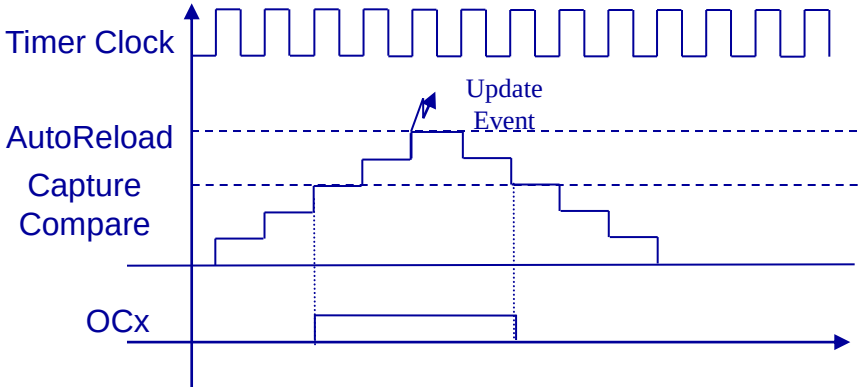
PWM Mode

- The PWM mode allows to generate:
  - 6 signals for TIM1 (3 independent signals + 3 complementary signals)
  - 1 signal for TIM2
  - 1 signal for TIM3
  - The frequency and the duty cycle determined as follow:
    - One auto-reload register to defined the PWM period.
    - Each PWM channel has a Capture Compare register to define the duty cycle.
- There are two configurable PWM modes:
  - Edge-aligned Mode
  - Center-aligned Mode

Edge-aligned Mode



Center-aligned Mode



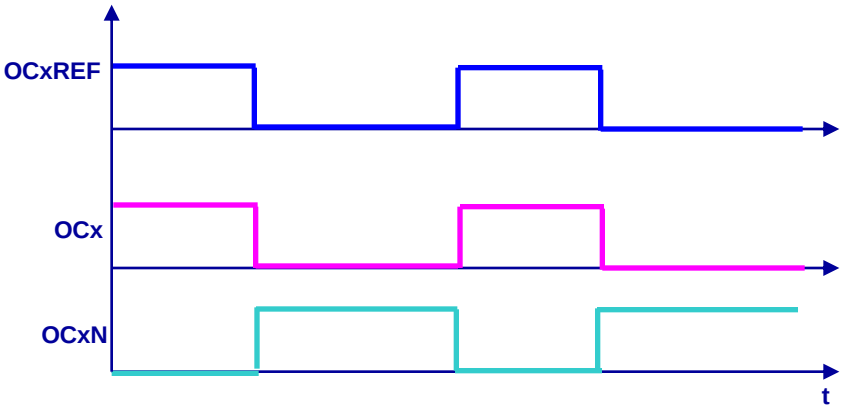
Complementary PWM outputs for motor control

- This mode allows the TIM1 to:
  - Output two complementary signals for each three channels.
  - Output three independent signals for each three channels.
  - Manage the dead-time between the switching-off and the switching-on instants of the outputs.
- One reference waveform OCxREF can generate 2 outputs OCx and OCxN for the three channels.
- Full modulation capability (0 and 100% duty cycle), edge or center-aligned patterns.
- Three programmable write protection levels:
  - Level1: Break configuration bits and output idle state 1 bits are locked.
  - Level2: Level1 + capture compare polarities and Off-state selection for run and Idle state are locked.
  - Level3: Level2 + Capture Compare control bits are locked.

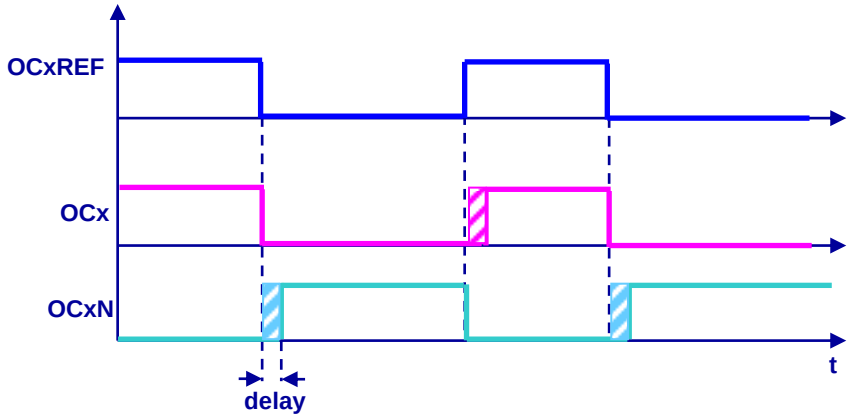
Complementary PWM outputs for motor control

Examples of OCx waveform in Complementary PWM mode

Dead-time disabled



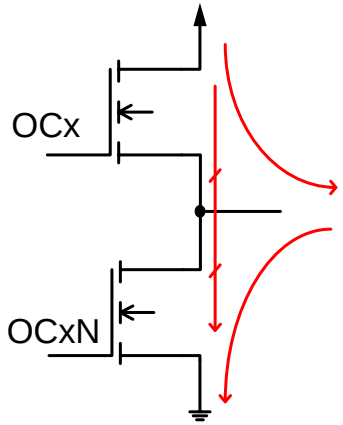
Dead-time enabled



Reference waveform OCxREF generates 2 outputs OCx and OCxN for the three channels:

- OCx rising edge is delayed to **reference rising** edge
- OCNx rising edge is delayed to **reference falling** edge

Dead-time is programmable to be adjusted depending on the characteristics of the devices connected to the outputs



The break function

- The break can be generated by:
  - The BRK input
  - The comparator 2 output
- When a break occurs:
  - The Main Output Enable bit (MOE) is cleared
  - Each output channel is driven with the level programmed in the OISx bit
  - The break status flag is set
  - An interrupt can be generated if the BIE bit is set.

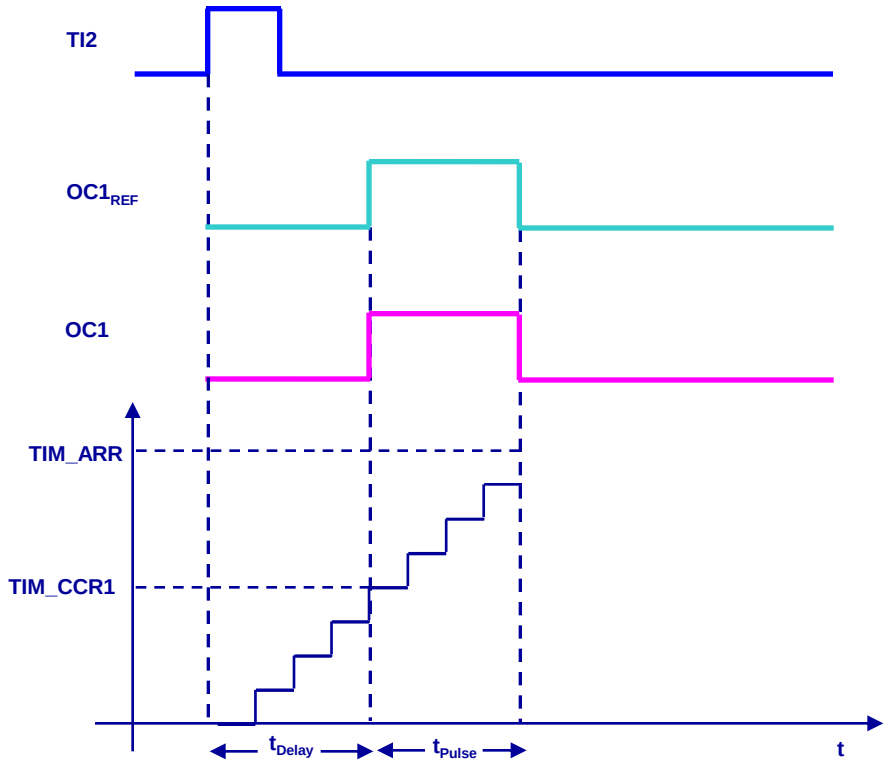
- Break applications:
  - If the Automatic Output Enable bit (AOE) is set, the MOE bit is automatically set again at the next update event UEV

    ⇨ In this case, it can be used to perform a regulation.
  - If the AOE is reset, the MOE remains low until you write it to '1' again

    ⇨ In this case, it can be used for security and you can connect the break input to an alarm from power drivers, thermal sensors or any security components.

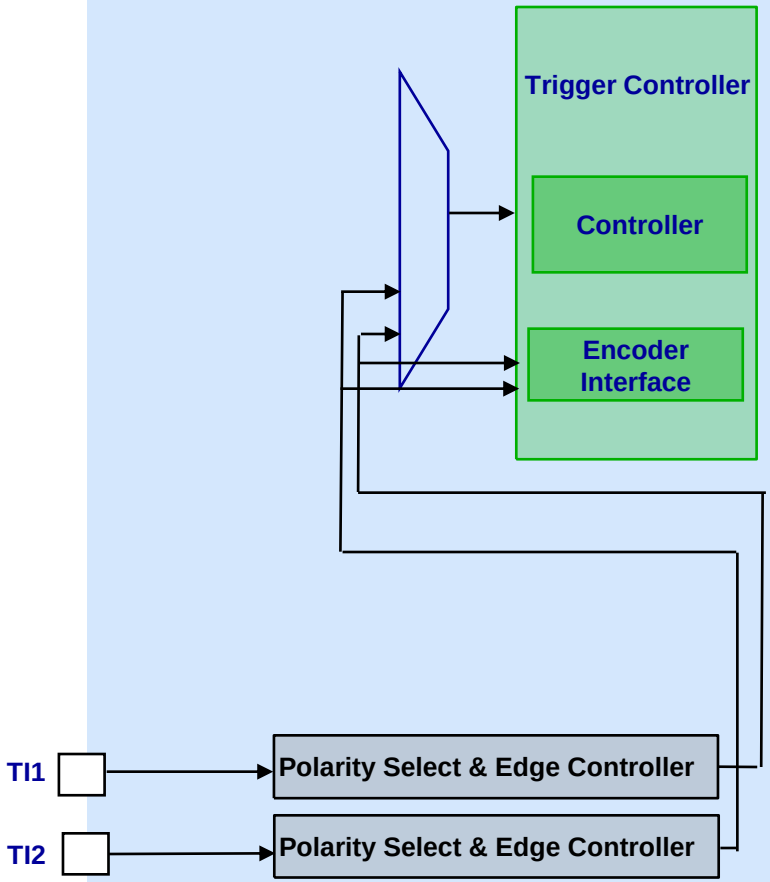
One Pulse Mode

- One Pulse Mode (OPM) is a particular case of the previous modes: Output Compare and Input Capture.
- It allows the counter to be started in response to a stimulus and to generate a pulse with a programmable length after a programmable delay.
- There are two One Pulse Mode waveforms selectable by software:
  - Single Pulse
  - Repetitive Pulse



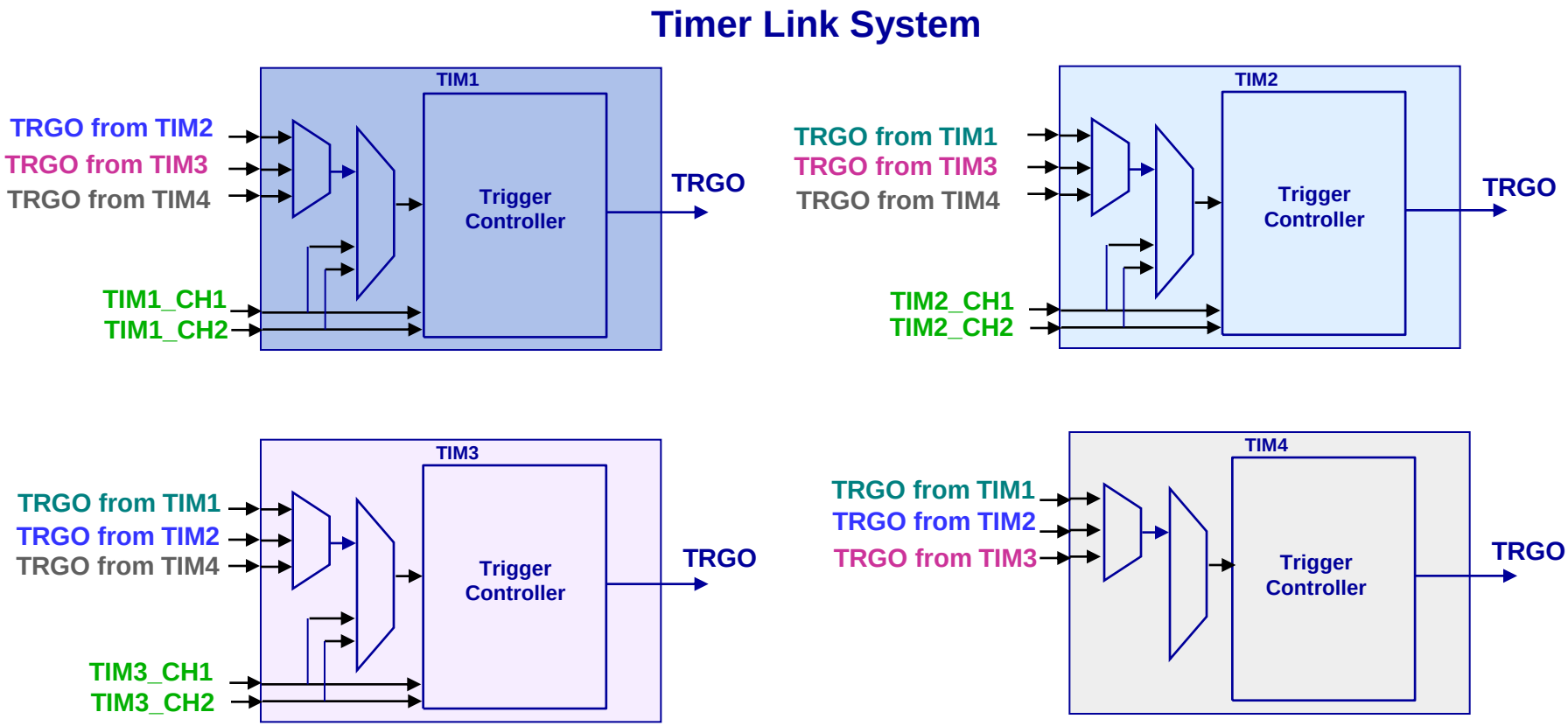
Encoder Interface

- Encoders are used to measure position and speed of motion systems (either linear or angular)
- The encoder interface mode acts as an external clock with direction selection
- The counter provides information on the current position (for instance angular position of an electric motor's rotor)
- To obtain dynamic information (speed, acceleration) you can measure the number of counts between two periodic events, generated by another timer
- Encoders and Microcontroller connection example:
  - An external incremental encoder can be connected directly to the MCU without external interface logic.
  - The third encoder output which indicates the mechanical zero position, may be connected to an external interrupt and trigger a counter reset.



TIMs Synchronization

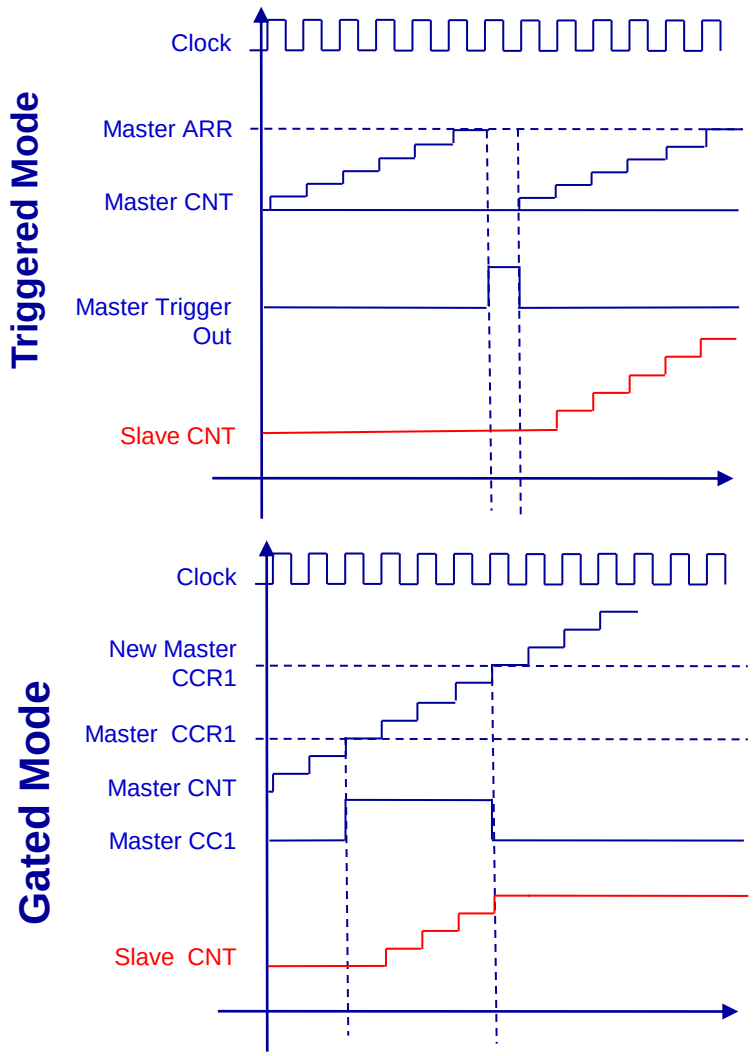
- The four Timers are linked together for timer synchronization or chaining.



Synchronization Mode Configuration

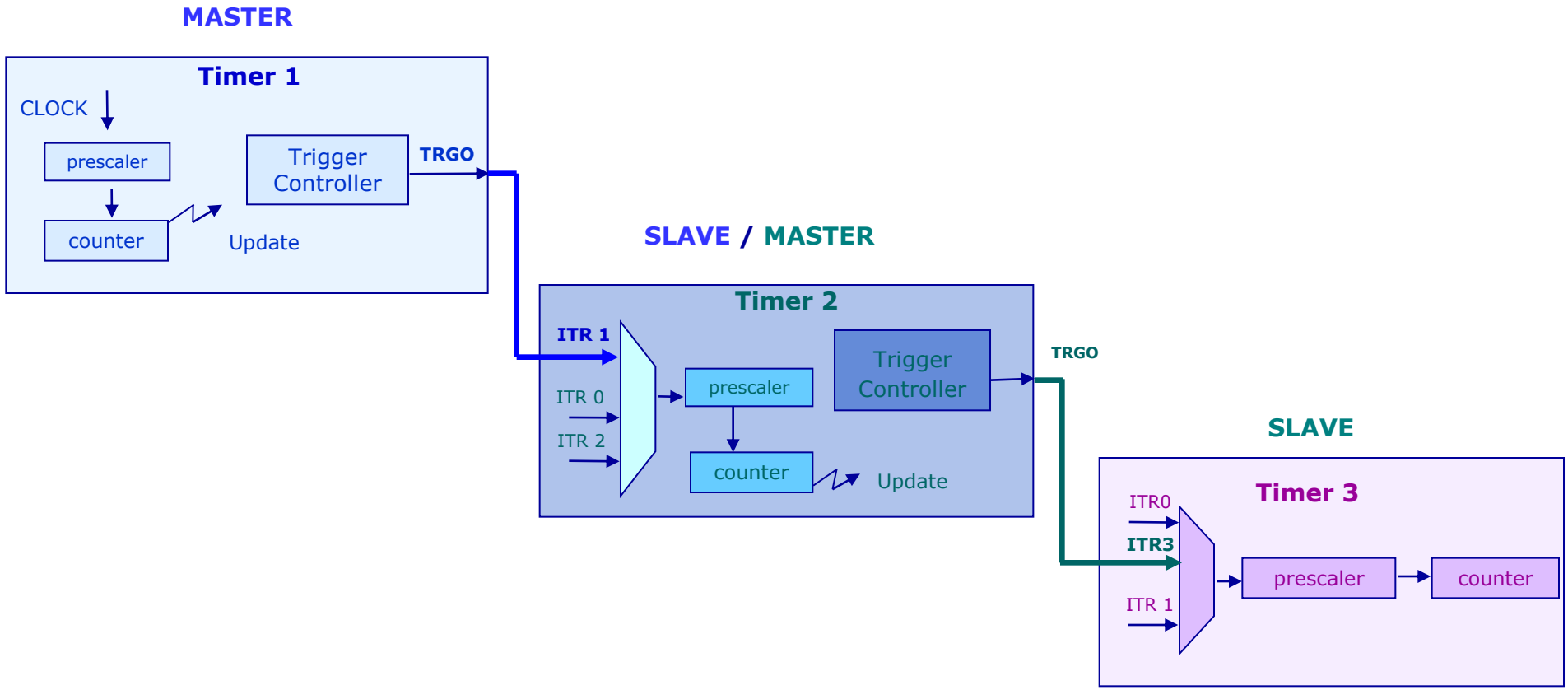
- The Trigger Output can be controlled on:
  - Counter reset
  - Counter enable
  - Update event
  - OC1 / OC1Ref / OC2Ref / OC3Ref

- The slave timer can be controlled in two modes:
  - Triggered mode : only the start of the counter is controlled.
  - Gated Mode: Both start and stop of the counter are controlled.



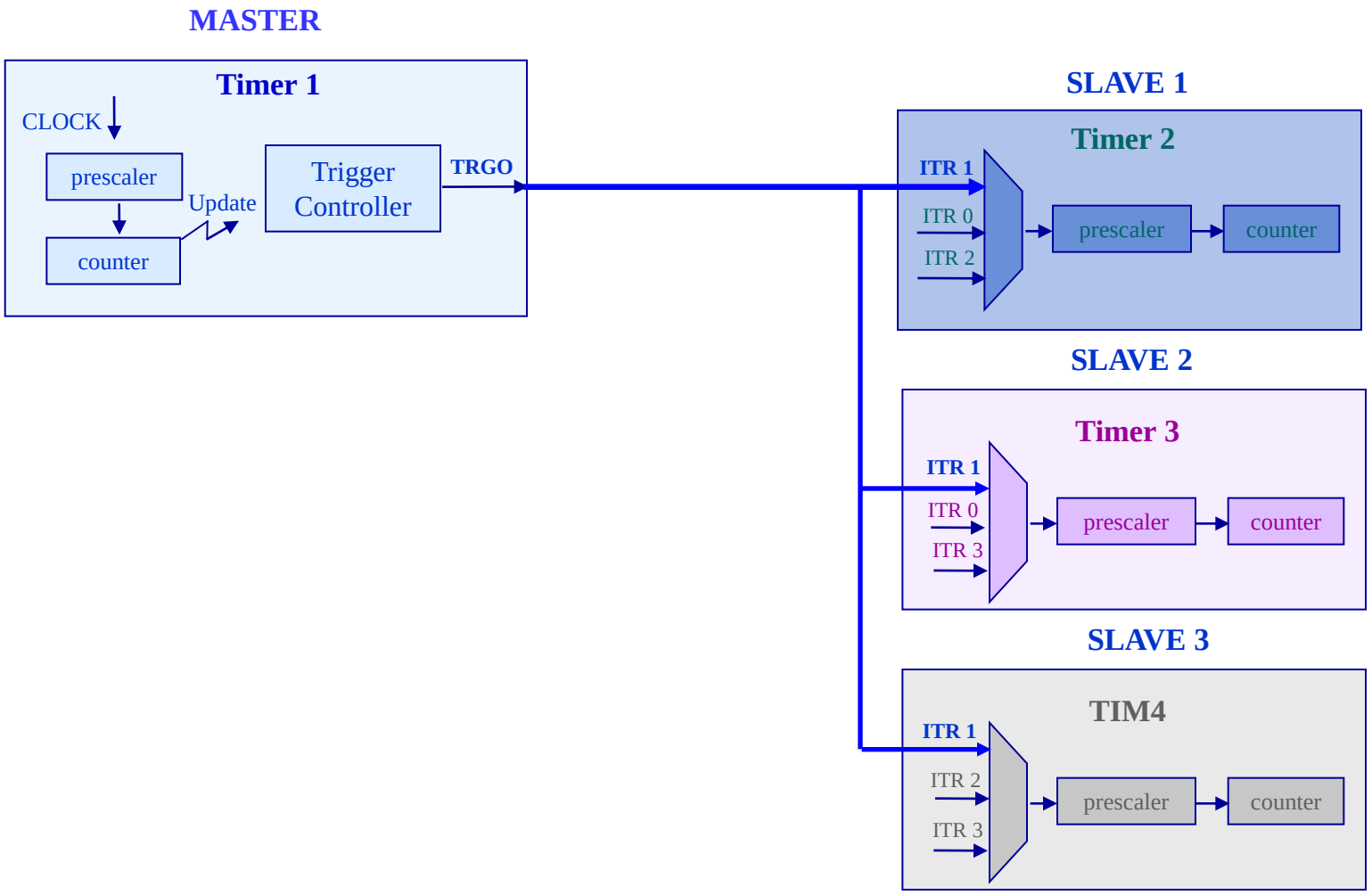
Synchronization – Configuration examples (1/3)

- Cascade mode:
  - TIM1 used as master timer for TIM2, TIM2 configured as slave for TIM1 and master for TIM3.



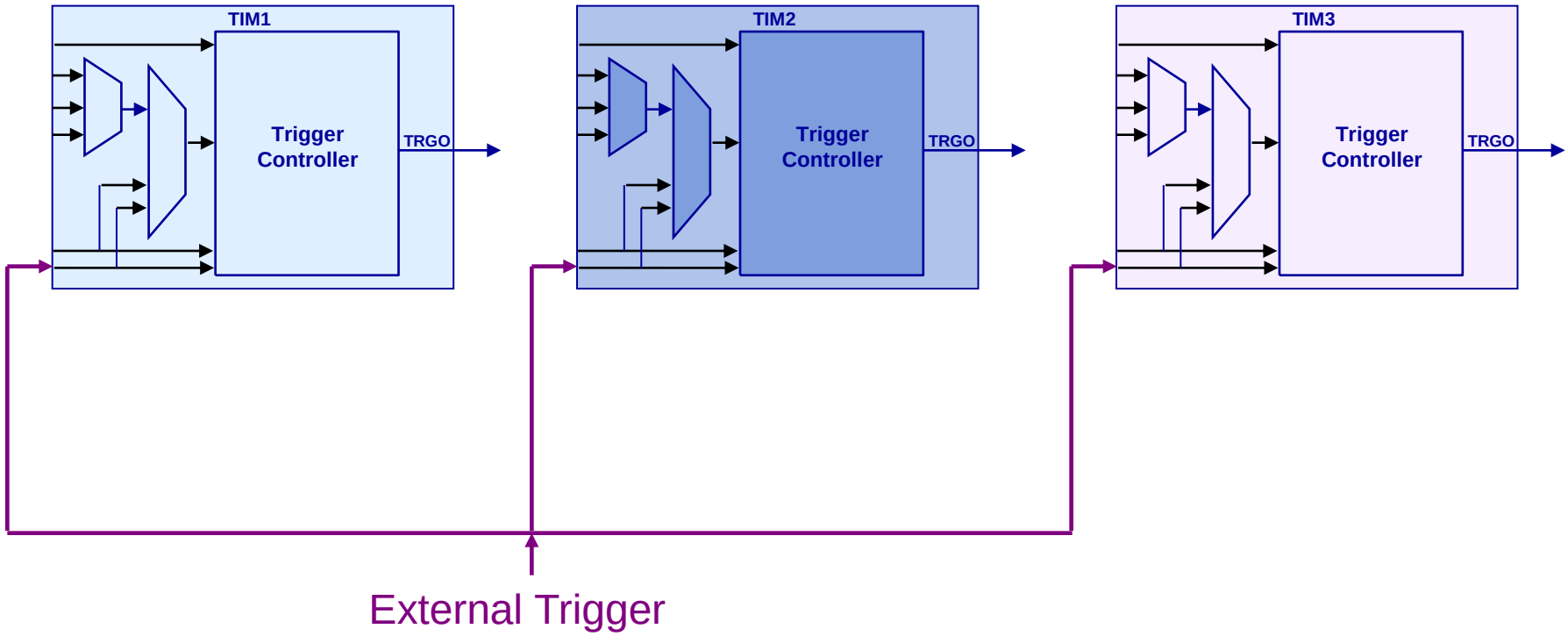
Synchronization – Configuration examples (2/3)

- One Master several slaves:
  - TIM1 used as master for TIM2, TIM3 and TIM4.



Synchronization – Configuration examples (3/3)

- Timers and external trigger synchronization
  - TIM1, TIM2 and TIM3 are slaves for an external signal connected to respective Timers inputs.



Timer features comparison

Timer	Counter type	Prescaler	Cap. Comp. Channels	Complem. outputs	Repet. counter	Ext. trigger / break inputs	Interrupt sources	DMA requests
TIM1(1) 16-bit advanced control timer	up/down	from 1 to 65536 (Any integer)	3+1(2)	3	Yes	Yes	Break Trigger Commutation Capture/Compare *i* Update event	Commutation Capture/Compare *I* Update event
TIM2 & **TIM3** 16-bit general purpose timers	up/down	from 1 to 128 (Any power of 2)	2	None	No	Yes	Break Trigger Capture/Compare *i* Update event	Capture/Compare *I* Update event
TIM4 8-bit basic timer	Up	from 1 to 32768 (Any power of 2)	0			No	Trigger Update event	Update event

(1) TIM1 is not present in STM8L101xx microcontrollers

(2) There are 4 capture/compare channels implemented but only 3 are connected to I/Os. The fourth channel can only be used to generate interrupt and DMA request.

Quiz

- How many timers there is in STM8l15x ?

- Which timer is dedicated to motor control ?

- How many channels there are for each timer ?

- How many synchronization modes there are between timers ?

- How many Interrupts and DMA requests supported by TIMs ?

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